SN74LVC1G17-EP

SGLS336A-APRIL 2006-REVISED JUNE 2007

SINGLE SCHMITT-TRIGGER BUFFER

FEATURES

- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Qualification Pedigree⁽¹⁾
- Supports 5-V V_{CC} Operation
- Max tpd of 4.6 ns at 3.3 V
- Low Power Consumption, 10 µA Max I_{CC}
- ±24 mA Output Drive at 3.3 V
- Ioff Supports Partial Power Down Mode
 Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

DESCRIPTION/ORDERING INFORMATION

This single Schmitt-trigger buffer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G17 contains one buffer and performs the Boolean function Y = A. The device functions as an independent buffer, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

NanoStar[™] and NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE	<u>=</u> (2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOT (SC-70) - DCK	Reel of 3000	SN74LVC1G17MDCKREP	C70
-55 C 10 125 C	SOP (SOT-23) - DBV	Reel of 3000	SN74LVC1G17MDBVREP	C170

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

INPUT A	OUTPUT Y
Н	н
L	L

FUNCTION TABLE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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• ESD Protection Exceeds JESD 22

- 2000-V Human-Body Model (A114-A)
- 200-V Machine Model (A115-A)
- 1000-V Charged-Device Model (C101)
- ⁽¹⁾ Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		VALUE	UNIT
V_{CC}	Supply voltage range	–0.5 to 6.5	V
VI	Input voltage range ⁽²⁾	–0.5 to 6.5	V
	Voltage range applied to any output in the high-impedance or power-off state	-0.5 to 6.5	V
Vo	Voltage range applied to any output in the high or low state ^{(2) (3)}	-0.5 to V _{CC} + 0.5	V
I _{IK}	Input clamp current (V _I < 0)	-50	mA
I _{OK}	Output clamp current (V _O < 0)	-50	mA
I _O	Continuous output current	±50	mA
	Continuous current through V _{CC} or GND	±100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾ : DCK package	252	°C/W
T _{stg}	Storage temperature range	-65 to 150	°C

LOGIC DIAGARAM (POSITIVE LOGIC)

 \rightarrow

<u>4</u> Y

A _____

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MAX	MAX	UNIT	
V	Supply veltage	Operating	1.65	5.5	V	
V _{CC}	Supply voltage	Data retention only	1.5		v	
VI	Input voltage		0	5.5	V	
Vo	Output voltage		0	V _{CC}	V	
		V _{CC} = 1.65 V		-4		
		V _{CC} = 2.3 V		-8		
I _{OH}	High	V 2.V		-16	6 mA	
	High	$V_{CC} = 3 V$		-24		
		$V_{CC} = 4.5 V$		-32		
		V _{CC} = 1.65 V		4		
		$V_{CC} = 2.3 V$		8		
I _{OL}	Low-level output current	V 2.V	16		mA	
		$V_{CC} = 3 V$		24		
		$V_{CC} = 4.5 V$		32		
T _A	Operating free-air temperature		-55	125	°C	

 All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, Implications of Slow or Floating CMOS Inputs (SCBA004).



ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V _{cc}	MIN TYP ⁽¹⁾	MAX	UNIT	
			1.65 V to 4.5 V	0.76	1.13		
			2.3 V	1.08	1.56		
V _{T+}	Positive-going input threshold voltage		3 V	1.48	1.92	V	
	theshold voltage		4.5 V	2.19	2.74		
			5.5 V	2.65	3.33		
			1.65 V to 4.5 V	0.35	0.59		
	Negative-going		2.3 V	0.56	0.88		
V _{T-}	input threshold		3 V	0.89	1.2	V	
	voltage		4.5 V	1.51	1.97		
			5.5 V	1.88	2.4		
&Delt			1.65 V to 4.5 V	0.36	0.64		
a;V <s< td=""><td></td><td></td><td>2.3 V</td><td>0.45</td><td>0.78</td><td></td></s<>			2.3 V	0.45	0.78		
ubscri pt>T </td <td></td> <td></td> <td>3 V</td> <td>0.51</td> <td>0.83</td> <td>V</td>			3 V	0.51	0.83	V	
Subsc	$(V_{T+} - V_{T-})$		4.5 V	0.58	0.93	3	
ript>			5.5 V	0.69	1.04		
		I _{OH} = -100 mA	1.65 V to 4.5 V	V _{CC} – 0.1			
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9		.,	
V _{ОН}		I _{OH} = -16 mA		2.4		V	
		$I_{OH} = -24 \text{ mA}$	3 V	2.3			
		I _{OH} = -32 mA	4.5 V	3.8			
		I _{OL} = 100 mA	1.65 V to 4.5 V		0.1		
		I _{OL} = 4 mA	1.65 V		0.45		
		I _{OL} = 8 mA	2.3 V		0.3	.,	
V _{OL}		I _{OL} = 16 mA	0.14		0.4	V	
		I _{OL} = 24 mA	3 V		0.55		
		I _{OL} = 32 mA	4.5 V		0.55		
1	A input	$V_1 = 5.5 \text{ or GND}$	0 to 5.5 V		±5	μA	
off		V_{I} or $V_{O} = 5.5 V$	0		±10	μA	
сс		$V_{I} = 5.5 \text{ V or GND}, I_{O} = 0$	1.65 V to 5.5 V		10	μA	
ΔI _{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V		500	μA	
C _i		$V_{I} = V_{CC}$ or GND	3.3 V	4.5		pF	

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}C$.

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SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)		TPUT)		V V _{CC} = 2.5 V ±0.2 V		V _{CC} = 3.3 V ±0.3 V		V _{CC} = 5 V ±0.5 V		UNIT
	(INPOT)	(001F01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	А	Y	2.8	9.9	1.6	5.5	1.5	4.6	0.9	4.4	ns

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	TER FROM TO (INPUT) (OUTPUT)	V _{CC} = 1.8 V ±0.15 V		V _{CC} = 2.5 V ±0.2 V		V _{CC} = 3.3 V ±0.3 V		V _{CC} = 5 V ±0.5 V		UNIT	
	(INFOT)	(001201)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	А	Y	3.8	11	2	6.5	1.8	5.5	1.2	5	ns

OPERATING CHARACTERISTICS,

 $T_A = 25^{\circ}C$

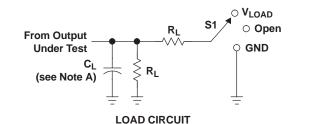
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	$V_{CC} = 2.5 V$	V _{CC} = 3.3 V	$V_{CC} = 5 V$	UNIT
	FARAMETER	TEST CONDITIONS	TYP	TYP	ТҮР	TYP	UNIT
\mathbf{C}_{pd}	Power dissipaton capacitance	f = 10 MHz	20	21	22	26	

Vı

0 V

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PARAMETER MEASUREMENT INFORMATION



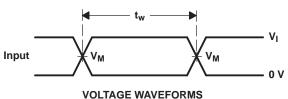
TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

VM

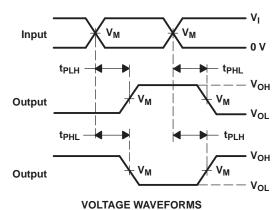
th

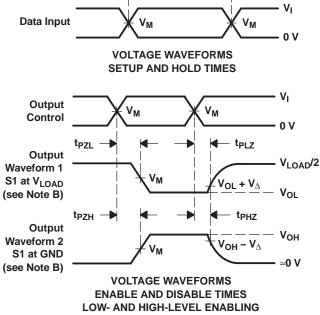
	INF	PUTS		V	•	-	N.
V _{CC}	VI	t _r /t _f	VM	V _{LOAD}	CL	RL	V_{Δ}
1.8 V \pm 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	$2 \times V_{CC}$	15 pF	1 Μ Ω	0.15 V
$\textbf{2.5 V} \pm \textbf{0.2 V}$	V _{CC}	≤2 ns	V _{CC} /2	$2 \times V_{CC}$	15 pF	1 MΩ	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V \pm 0.5 V	V _{CC}	≤2.5 ns	V _{CC} /2	$2 \times V_{CC}$	15 pF	1 Μ Ω	0.3 V

Timing Input



PULSE DURATION





t_{su}

PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

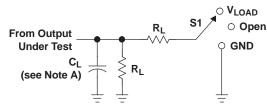
- NOTES: A. $\ensuremath{\mathsf{C}}_L$ includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω .
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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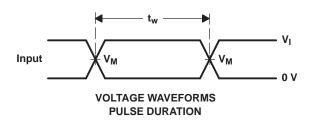
PARAMETER MEASUREMENT INFORMATION (continued)



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND



N	INF	PUTS	N	N	•		N
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	RL	V_{Δ}
1.8 V \pm 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2 × V _{CC}	30 pF	500 Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V \pm 0.5 V	V _{CC}	≤2.5 ns	V _{CC} /2	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



٧_M

Vм

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

INVERTING AND NONINVERTING OUTPUTS

Vм

Vм

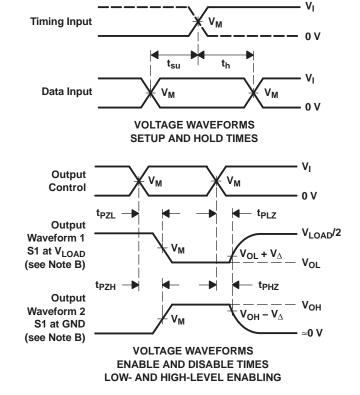
Input

Output

Output

t_{PLH}

t_{PHL}



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.

V

0 V

– V_{OH}

VoL

VOH

 V_{OL}

t_{PHL}

tPLH

Vм

Vм

- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC1G17MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G17MDCKREP	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06621-01XE	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06621-01YE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G17-EP :

Catalog: SN74LVC1G17

Automotive: SN74LVC1G17-Q1

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G17MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G17MDCKREP	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3



PACKAGE MATERIALS INFORMATION

21-Aug-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G17MDBVREP	SOT-23	DBV	5	3000	195.0	200.0	45.0
SN74LVC1G17MDCKREP	SC70	DCK	5	3000	195.0	200.0	45.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

D. Falls within JEDEC MO-178 Variation AA.



DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.



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